REMARKS

Applicants respectfully request the Examiner's reconsideration of the present application as amended. Claims 13, 14, 16-23 remain in the application. Claim 15 has been canceled. Claim 13 has been amended. Claims 21 –23 have been added.

Claims 13-20 were rejected under 35 U.S.C. § 102(e) as being anticipated by Maloney (6,269,199 B1), with a publication/issue date of July 31, 2001. The present application is a Divisional of Application No. 09/649,716, filed on August 28, 2000, which claims the benefit to Provisional Application No. 60/151,814 filed on August 30, 1999. The Applicants respectfully submit that since the effective filing date of the present divisional application is July 21, 2003, 35 U.S.C. § 103(c) operates to bar the use of Maloney as prior art in any possible rejections based on non-obviousness.

Maloney discusses integrated circuits comprised of an array of MOSFET elements to form through silicon optical modulators (TSOM) that cause optical phase shifts of reflected light in order to identify a state of a signal (Maloney, Abstract).

Claim 13 as amended, claims:

> A method of making a symmetric transistor device comprising:
> depositing a first conductive layer on a substrate, the first conductive layer forming an even number of transistor legs, laid out in an intersecting pattern, forming a bilaterally symmetric base;
> doping the substrate to form source and drain regions and forming non-diffused areas around the intersections of the transistor legs; and
> forming a plurality of transistors defined by a portion of a transistor leg forming a gate and the source and drain areas on either side of the leg forming a source and a drain.

Applicants respectfully submit that Maloney does not disclose undoped areas around the intersections of the transistor legs. The Office Action suggests that Maloney anticipates this claim since the regions covered by the gate grid remain undoped. The

Office Action refers to the channel region directly beneath the transistor gate 402, as shown in Maloney's Fig. 6B, as an example of an undoped region.

Maloney's Fig. 6B shows a cross-section image of an optical modulator 400 (Maloney, column 7, line 63). The modulator is fabricated using a p-doped substrate 406 in which an n-doped isolation well 410 is provided (Maloney, column 7, lines 63-65). The grid 402 includes a plurality of source/drain regions 404 (Maloney, column 8, lines 6-7). In MOSFET technology, the channel region directly beneath a transistor gate is also doped, and there is a layer of metal oxide underneath the gate that separates the gate from the semiconductor. Maloney teaches such a MOSFET structure (Maloney, column 5, lines 19-23). The Applicants respectfully submit that therefore Maloney does not teach any undoped areas around the intersections of the transistor legs.

Applicants further submit that newly added claim 21 and dependent claims 22 and 23 are not anticipated by Maloney since Maloney does not teach that the gate orientation reduces skew effects due to mask alignment and gate orientation.

Thus, Applicants respectfully submit that in view of the amendments and discussion set forth herein, the applicable rejections have been overcome. Accordingly, the present and amended claims should be found to be in condition for allowance.

If a telephone interview would expedite the prosecution of this application, the Examiner is invited to contact Judith Szepesi at (408) 720-8300.

If there are any additional charges/credits, please charge/credit our deposit account no. 02-2666.

Respectfully submitted,
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